Are Trench FETs Too Fragile for Linear Applications?

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A comparison of the forward-biased safe-operating-area (FB-SOA) performance of one trench and one planar device of similar die size is presented. The results educate designers on issues concerning trench and planar MOSFETs in the linear region of the device operating characteristics.

Most electronics designers wouldn't be surprised to hear that trench FETs are less robust than planar FETs in forward-biased safe-operating area (FB-SOA). The comparison normally would be between devices of similar $R_{ds\text{-}on}$, and the trench device would have a much smaller die than the planar device. It would be easy to dismiss SOA differences based largely on the smaller die, and hence lower thermal mass and higher thermal resistence.

The focus of this discussion is operation in the linear region of the device-operating characteristic. That is, the device isn't in the resistive (V_{ds}/I_{ds}) region commonly used in switching applications. Instead, it's operating in the "constant current" (saturated) region of the FET characteristic, where the current is largely a function on the gate-source voltage. This is the operating region of a device used as a pass-element in a linear regulator, in a linear amplifier or as an active clamp. It's also the operating region for vari-

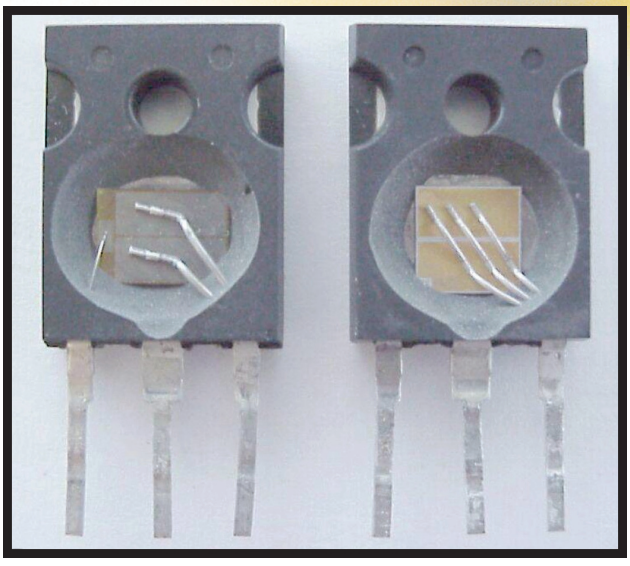

Fig. 1. *Planar (left) and Trench (right) test FETs with their die exposed.*

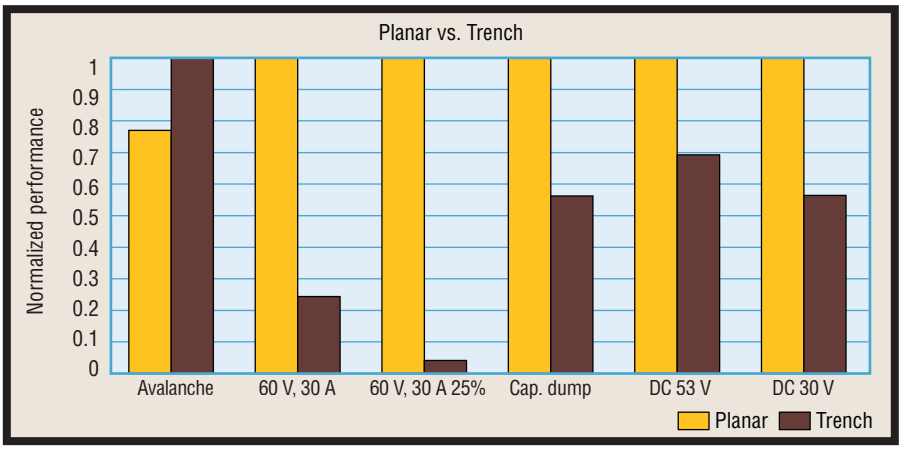

Fig. 2. *Comparison of the performance of Planar vs. Trench FETs for the various tests. The results are normalized, with 1 being the performance of the better-performing part.*

ous fault conditions (such as short-circuited outputs) or when charging capacitors through a FET switch, etc.

The devices come from two different manufacturers. Both devices are packaged in TO-247 packages and exhibit very similar steady-state thermal resistance. The planar part has a 51-mm^2 die area and is rated at 150 V. The trench part has a 47.6-mm^2 die area and is rated at 110 V. The $R_{ds\text{-}on}$ for planar device is approximately three times the $R_{ds\text{-}on}$ of the trench part. **Fig. 1** shows photographs of the test parts with their die exposed.

The tests were tailored for a specific application. This application uses the FET as a series-pass element to provide a very-low-resistance power-path for normal operation. During various input overvoltage conditions, the FET operates in the linear region to drop voltage and to limit the voltage provided to the load side of the circuit. The rationale for the individual tests won't be described, but each test will be described. Avalanche capability also was tested as a point of comparison between the parts.

Trench vs. Planar

The tests include:

● *Avalanche.* A 1-mH inductor provided avalanche energy to the part. Initial inductor current (energy) was gradually increased until the part failed.

● *30-A, 60-V continuous.* The part was operated at 30 A and 60 V until failure. The time-to-failure was used as an indicator of the part's tolerance of this condition.

● *30 A, 60 V (300-µs on, 900-µs off.* This is like the previous test. However, the parts were run at a 25% duty cycle to decrease the average power but still operate the part in a reasonably high-current/high-voltage part of its operating characteristic. The number of cycles-to-failure was used as an indicator of the part's tolerance of this condition.

● *Capacitor dump.* A 4300-µF capacitor was precharged to a test voltage and then discharged through the test device at a constant V_{gs}. The precharge voltage was increased in increments of 5 V, and the test repeated until the device failed. This was done at several different gate voltages and achieved similar results. Only the results for V_{gs} of 5 V will be reported here.

● *Static dc.* The device was mounted on a 20°C liquid-cooled cold-plate and operated at a predetermined V_{ds}. The I_{ds} was increased in small increments, allowing time for thermal stabilization between steps. This was continued until the part failed. The power level just prior to failure is used as the indicator of part capability in this test. Peak stable die temperature prior to failure is also reported. This article only covers a subset of this testing. The results reported here are with a thermal interface of only thermal grease, no insulator. This yielded a thermal resistance of about 0.6°C/W from junction to coolant.

The results are described below for each test and are charted in **Fig. 2**.

● *Avalanche.* This was the one area where the trench part outperformed the planar part. This might be antici-

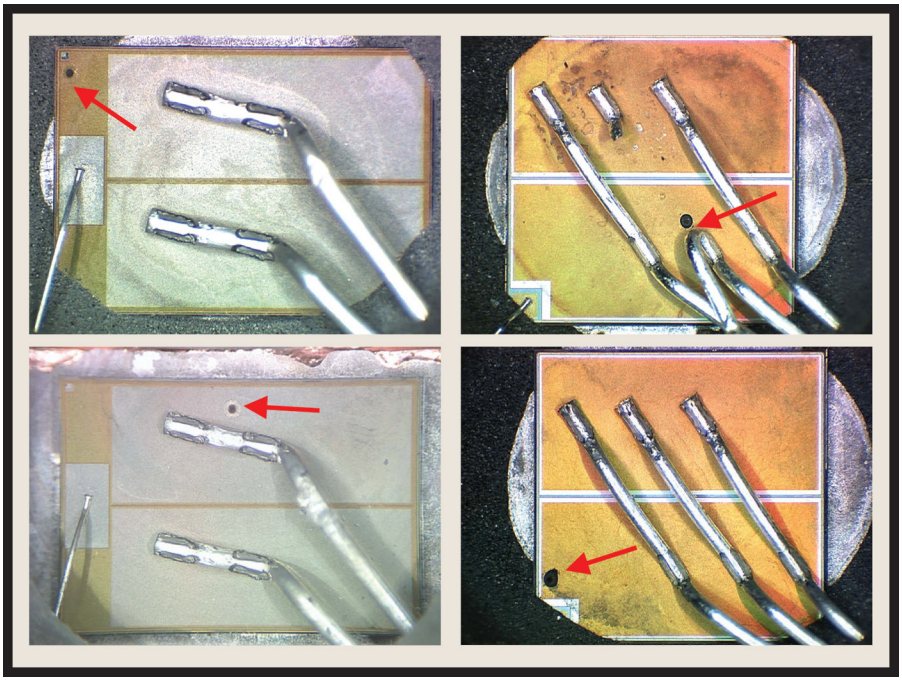

Fig. 3. *Avalanche damage to Planar FETs (left) and Trench FETs (right). The bond-wire has been cut and moved out of the way to expose the damage in the part at upper right.*

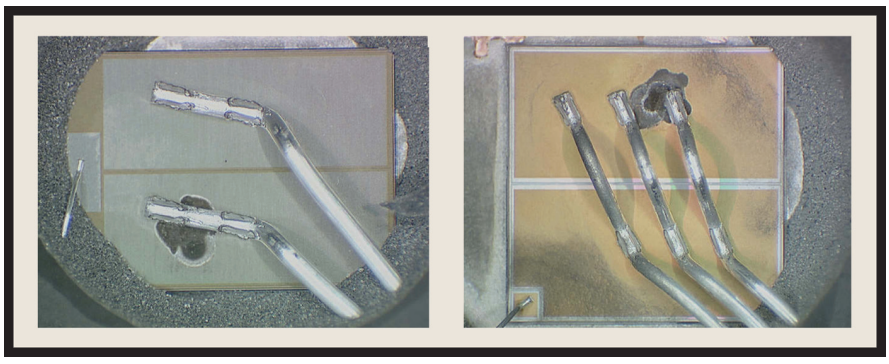

Fig. 4. *FETs destroyed by the 30 A, 60 V, continuous test. Planar is on the left; Trench is on the right.*

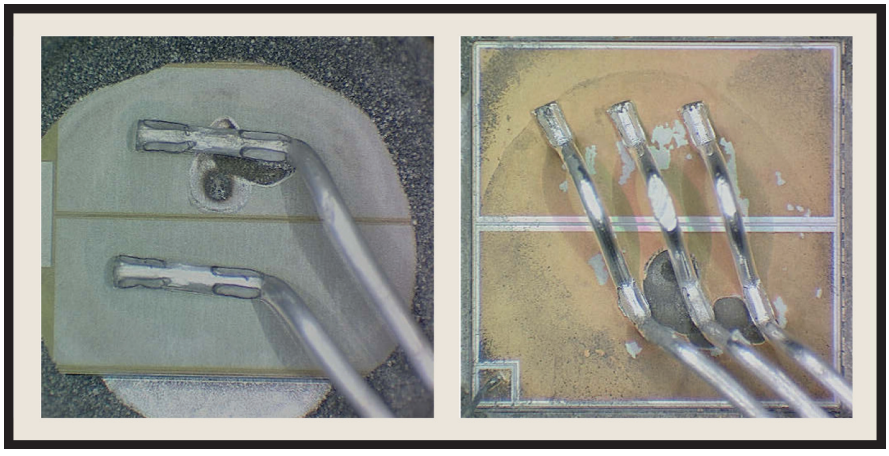

Fig. 5. *FETs destroyed by the 30 A, 60 V, 25% duty-cycle test. Planar is on the left; Trench is on the right.*

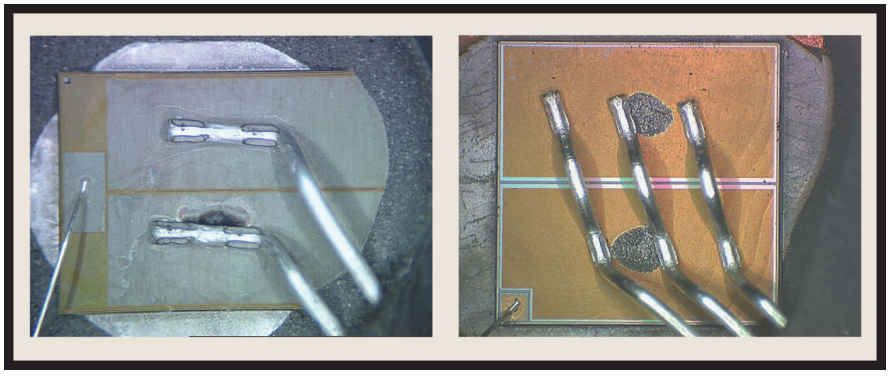

Fig. 6. *FETs destroyed by the capacitor-dump test. Planar is on the left; Trench is on the right. Note the dual damage sites on the trench part.*

pated because of the difference in voltage rating of the parts. However, other factors may also affect this result. The trench parts failed at an average of 4.6 joules. The planar parts failed at an average of 3.6 joules.

Avalanche damage tended to be located randomly on the die for both the planar and trench parts. **Fig. 3** shows photographs of avalanche damage to each type of part.

● *30-A, 60-V continuous.* Planar parts failed at an average of 2555 µs, while the trench parts failed at an average of 624 µs. The damage site was consistently adjacent to and between wire bonds. **Fig. 4** depicts damage caused to the FETs by this test.

● *30 A, 60 V (300-µs on, 900-µs off).* While the planar FETs failed at an average of 72.5 pulses, the trench parts failed on the third pulse. The damage site was consistently adjacent to and between wire-bonds. **Fig. 5** shows examples of the resulting FET damage.

● *Capacitor dump.* Planar failed at a capacitor precharge voltage of 60 V. The trench failed at a capacitor precharge voltage of 45 V. This is reported as an initial capacitor energy value: 7.74 joules for the planar part and 4.35 joules for the trench transistor. As shown in **Fig. 6**, the damage site was consistently between wire bonds. The figure indicates that the trench FET can have two damage sites.

● *Static dc.* This result is possibly the most alarming. Using V_{ds} of 53 V, the average planar part survived a dc operating condition of 132.6 W and failed to withstand a 5.3-W increase. Peak die temperature at the last stable operating point before destruction averaged 129°C, well within the published maximum allowed junction temperature. The average trench part survived 91.9 W and failed to withstand a 5.3-W increase. Peak die temperature at the last stable operating point before destruction averaged a mere 90°C. The attempted power increase could reasonably have been expected to produce an increase of only ~5°C on both devices. Using a V_{ds} of 30 V produced the following results: The planar part failed beyond the 176-W point, failing to withstand a 3-W increase. The trench part failed beyond 99 W, failing to withstand a 3-W increase. Peak die temperatures at the last stable operating point before destruction was 183°C and 103°C, respectively. **Fig. 7** illustrates the damage to each type of FET for the 53-V test condition. **Fig. 8** shows corresponding thermographs at the last stable operating point before the parts failed.

Examining Device Failure

Both the planar and the trench MOSFETs showed formation of hot spots in the dc testing, and ultimately exhibited thermal-runaway and device failure beginning at die temperatures (both peak and average) far below what would be expected when

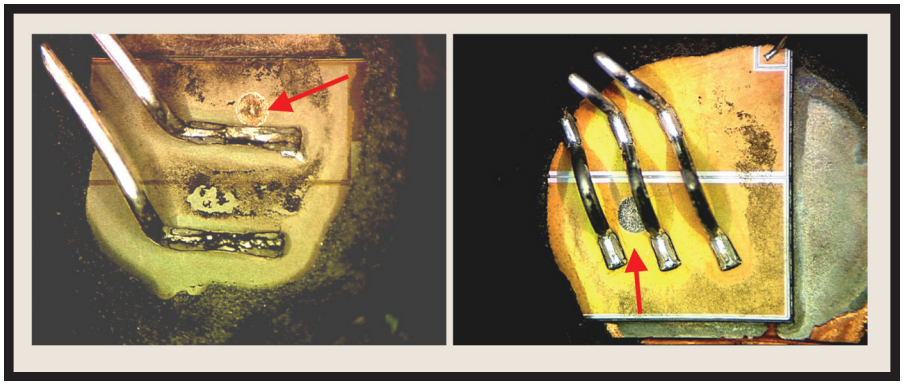

Fig. 7. *FETs destroyed by the static DC test at 53 V. Planar is on the left; Trench is on the right.*

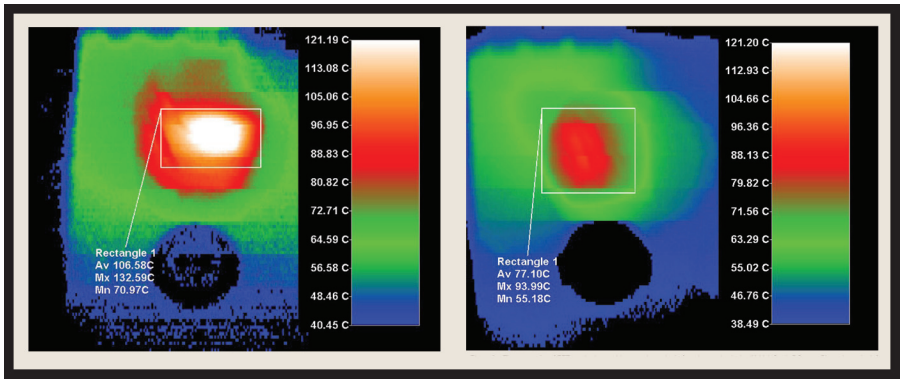

Fig. 8. *Thermographs of FETs at the last stable operating point before destruction in the 53-V static DC test. Planar is on the left; Trench is on the right.*

using traditional application principles. This hot-spot/runaway phenomenon is highly dependent on the thermal system and the operating point. Further testing has shown that the insertion of additional thermal resistance in the interface between the FET case and the cold-plate (such as Sil-Pad) allows the device to operate at far higher temperatures (but not power) before the onset of runaway. This is presumably because of the improved thermal cross-coupling between FET cells—the FET case (for example, tab) acts more effectively as a thermal-spreader when the thermal resistance to the heat sink is increased. Hence, the deviation from the classically predicted dc SOA is far more dramatic with a high-performance thermal system because of less thermal cross coupling between cells. The runaway phenomenon is also more prevalent at higher drain-source voltages (resulting in a higher dP/dT for a given device dI_d/dT).

Thermal runaway within FETs has been reported and analyzed in literature [1,2,3]. These papers address the cause of the phenomenon and address some analysis techniques that apply to runaway during transient events (where the device thermal masses dominate the results). Yet this effect doesn't seem to be well known among designers, and the data from semiconductor suppliers often doesn't suggest there is any issue to be considered, especially with dc SOA. It's obvious to designers that high-voltage/high-current linear modes of operation have serious thermal limitations. However, it's less intuitive that high-voltage/low-current linear modes can be more susceptible to failure.

Use of published device data (SOA and transient thermal impedance) typically relies strongly on assumptions of isothermal operation—which clearly isn't the case in our dc tests and is probably not the case in other forward-biased tests. Application of SOA data as-published may result in a significant potential for unexpected device failure, especially in the operating area that is often not covered in SOA curves, such as the longer pulse durations and dc operation. Some published trench device SOA data shows lower power/energy capability at the higher voltages and longer pulse widths, with some SOA curves also including a dc line—sometimes at as little as 15% of the capability near the $R_{ds\text{-}on}$ line. Even with the derated curves, adaptation of these curves to a specific application may not be possible, with the thermal system being a significant variable that can't be reasonably accounted for, at least at long pulse durations and dc operation. Note that the results reported here are at 60 V and below—still some distance from the rated voltages of 150 V and 110 V. Actual testing that shows low die temperatures may be of little assurance, since the part could be on the verge of thermal runaway.

Hot-spot/ runaway phenomena within a device are somewhat analogous to power-sharing issues when discrete FETs are paralleled. Designers often assume FETs share power well when paralleled because of the positive temperature coefficient of $R_{ds\text{-}on}$ when the devices are operating in the resistive region. This positive temperature coefficient tends to decrease any imbalance between devices. But when paralleled FETs are operated in the linear region, they don't necessarily share power well.

The threshold voltage has a negative temperature coefficient, which tends to exaggerate any imbalance between devices at any operating point close to the threshold voltage (dI_d/dT is the actual parameter of interest—positive values exaggerate imbalance). Depending on the drain-source voltage, thermal impedance and thermal cross-coupling of the devices, this effect may become regenerative, causing thermal runaway. The effect is less of an issue at high drain currents, where the negative temperature coefficient of the transconductance can more than compensate for the threshold-voltage effect, resulting in a negative dI_d/dT.

The hot-spot phenomenon was far more dramatic with the trench part, presumably because of a higher positive temperature coefficient of I_d at the operating point, resulting in runaway at lower temperatures/power levels.

The other linear-mode tests showed the trench device is more easily destroyed than the planar part. The location of the damage site adjacent to a wire bond supports the notion that the hot spots are consistently located beside a wire bond where $I^*R_{source\text{-}metal}$ de-biasing is minimized.

The planar part failed the 60-V, 30-A test at about the time that would be predicted by the published transient thermal impedance data for that part. The published SOA data for this part shows only lines of constant power (for example, there isn't any "derating" at the higher drain-source voltages). This would suggest that the hot spot may not be a significant factor in this failure. The much earlier failure of the trench part in similar circumstances suggests that the hot-spot phenomenon is significant for the trench device.

Nothing clearly indicates if thermal runaway is a factor in the 60-V, 30-A tests (both at 100% and 25% duty cycles), but runaway should be less likely to occur at these higher currents than at the conditions used for the dc testing. The capacitor-dump results suggest a significant hot-spot issue, but the damage on the trench die in multiple locations in some instances appears to indicate a lack of runaway in this test. The very high current in the dump test makes runaway unlikely. The thermal system that the devices were connected to wasn't important in any of these tests—the device thermal masses apparently were dominant for these shorter events.

This hot-spot/runaway phenomenon also suggests reason for concern when using FETs with temperature-sensing diodes on the die. If the sense elements aren't in the hot spot of the die, they may not properly perform their protective function. Additionally, the hot spots may not always form in the same place on the die. The hot spots always formed near a wire bond, but not a specific wire bond.

One additional question to ask is why a designer would even consider using trench FETs in a linear application. The $R_{ds\text{-}on}$ advantage of trench wouldn't seem to be important for linear use. There are several possible answers to this question. First, a trench part might already be qualified and in production in another application, and the designer might simply be avoiding releasing parts unique to a new application. Or, the part might be used as a "relay" or switch where on-resistance is of concern during normal operation, but linear operation occurs during fault conditions or while charging capacitors during power-up.

In this latter case, there is a high risk that the designer would select a trench part with a smaller die size than an alternative planar part, compounding the problem. Finally, there's the possibility that the designer is unaware of the difference between these FET technologies or the strengths or weaknesses that go with them.

One additional note of caution: Reviewing a significant number of published FET datasheets reveals many thermal impedance graphs and SOA graphs with significant errors. Sometimes, the thermal impedance data doesn't agree at all with the SOA data on the same datasheet. In other cases, the data isn't consistent with other devices of similar die size, package-type and die attach method. Even where the SOA graphs may be correct, some devices (planar and trench) that show no voltage derating in the SOA graphs are prone to thermal runaway at dc and durations longer than shown in the SOA graphs. As noted earlier, even SOA graphs that include longer durations and dc can't be applied to a different thermal system for those longer durations.

Conclusion

Beware of trench FETs operating in the linear mode. Published SOA data may not be adequate to determine safe use in your specific application. Also, published SOA data may be incorrect. Therefore, it's recommended that testing is performed using a representative thermal system and operating conditions beyond those required by the application.

Also, beware of any FETs operating in linear mode for long pulse durations or dc—specially, if the operating point is in the higher-voltage and lower-current portion of the operating characteristic (such as far from the $R_{ds\text{-}on}$ line). **PETech**

Acknowledgments

The author would like to thank Rick Rouser for taking much of the data in this study. Thanks also to Bob Campbell for his assistance in numerous aspects of this study.

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